

IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Original) A delay circuit comprising:

a first switch connected between a first power supply and a first node, the first switch being switched according to an input signal;

a second switch having a current path connected at a first end thereof to the first node, the second switch being switched according to the input signal;

a third switch connected between a second end of the current path of the second switch and a second power supply, the third switch making a constant current flow according to a control signal formed of a constant current;

a capacitor connected between the first node and the second power supply; and

a differential amplifier supplied at a first input end thereof with a potential at the first node and supplied at a second input end thereof with a potential depending upon the control signal, the differential amplifier comparing the potential at the first node with the potential depending upon the control signal and outputting an output signal from an output terminal thereof.

2. (Original) The circuit according to claim 1, the differential amplifier comprising:

a fourth switch having a current path connected at a first end thereof to the first power supply;

a fifth switch having a current path connected at a first end thereof to a second end of the fourth switch and connected at a second end thereof to the second power supply, the fifth switch being connected at a gate thereof to the first input end;

a sixth switch having a current path connected at a first end thereof to the first power supply, the sixth switch being connected at a gate thereof to a gate of the fourth switch and a second end of the current path of the fourth switch; and

a seventh switch having a current path connected at a first end thereof to a second end of the sixth switch and connected at a second end thereof to the second power supply, the seventh switch being connected at a gate thereof to the second input end.

3. (Original) The circuit according to claim 1, further comprising a constant current source circuit for generating the control signal formed of the constant current.

4. (Original) The circuit according to claim 3, the constant current source circuit comprising:

a first current mirror circuit;

an eighth switch having a current path connected at a first end thereof to the first power supply, the eighth switch being connected at a gate thereof to an output node of the first current mirror circuit; and

a ninth switch having a current path connected at a first end thereof to a second end of the eighth switch, the ninth switch being connected at a second end of the current path to the second power supply, the ninth switch being connected at a gate thereof to the second end of the eighth switch, a gate of the third switch, and the second input end of the differential amplifier,

wherein the eighth switch and the ninth switch form a second current mirror circuit, the second current mirror circuit making a current equivalent to an output current of the first current mirror circuit flow.

5. (Original) The circuit according to claim 1, further comprising a latch circuit for holding the output signal of the differential amplifier.

6. (Original) The circuit according to claim 5, further comprising a first logic circuit having first and second input terminals and a first output terminal, an input signal and a control signal generated in response to a power supply voltage being supplied to the first and second input terminals, respectively, and the first output terminal being connected to gates of the first and second switches.

7. (Currently Amended) The circuit according to claim [[6]] 2, further comprising:

a latch circuit for holding the output signal of the differential amplifier;

a first logic circuit having first and second input terminals and a first output terminal, an input signal and a control signal generated in response to a power supply voltage being supplied to the first and second input terminals, respectively, and the first output terminal being connected to gates of the first and second switches.

a second logic circuit having third and fourth input terminals and a second output terminal, the third and fourth input terminals being supplied with an output signal of the first logic circuit and an output signal of the latch circuit;

~~a tenth~~ an eighth switch having a current path connected at a first end thereof to the first power supply and connected at a second end thereof to first ends of the fourth and sixth switches, a gate of the ~~tenth~~ eighth switch being supplied with an output signal of the second logic circuit; and

~~an eleventh~~ ninth switch having a current path connected at a first end thereof to second ends of the fifth and seventh switches and connected at a second end thereof to

~~ground~~ the second power supply, a gate of the ~~eleventh~~ ninth switch being supplied with an inverted output signal of the second logic circuit.

8. (Currently Amended) The circuit according to claim 7, the latch circuit comprising:
tenth, eleventh and twelfth switches connected in series between the first power supply and the second power supply, a connection node between the tenth and the eleventh switches being connected to an output node of the differential amplifier, the tenth and the eleventh switches being controlled by an output signal of the first logic circuit;

thirteenth and fourteenth switches connected in series between the first power supply and the second power supply, the thirteenth and fourteenth switches being controlled by the output signal of the differential amplifier, a potential at a connection node between the thirteenth and fourteenth switches controlling the twelfth switch; and

a fifteenth switch connected between the connection node between the thirteenth and fourteenth switches and the first power supply, the fifteenth switch setting the connection node between the thirteenth and fourteenth switches equal to a constant potential when the power supplies are turned on.

9. (Currently Amended) The circuit according to claim 8, wherein each of the first, fourth, sixth, eighth, ~~eleventh, fifteenth and seventeenth~~ tenth, thirteenth and fifteenth switches comprises a MOS transistor of first conductivity type, each of the second, third, fifth, seventh, ninth, ~~tenth, eleventh, thirteenth, twelfth and~~ fourteenth and sixteenth switches comprises a MOS transistor of second conductivity type, and each of the third, fourth, fifth, sixth, seventh, eighth, ninth and ~~fifteenth~~ thirteenth MOS transistors being set equal to substantially 0V in threshold voltage.

10. (Original) A delay circuit comprising:

- a first switch performing switching between a first power supply and a first node;
- a second switch performing switching between a second power supply and the first node;
- a capacitor connected at a first end thereof to the first node;
- a constant current source having an output terminal for outputting a constant current;
- a first MOS transistor of second conductivity type having a source, a drain and a gate, the first MOS transistor being included in a circuit of the constant current source, the drain and the gate being connected in common to the output terminal, the source being connected to the second power supply; and
- a current mirror differential amplifier for comparing a voltage at the first node with a voltage at the output terminal, the current mirror differential amplifier outputting a result of the comparison from a first output terminal.

11. (Original) The circuit according to claim 10, the differential amplifier comprising:

- second and third MOS transistors of first conductivity type having sources connected in common to the first power supply and having gates connected in common;
- fourth and fifth MOS transistors of second conductivity type having sources connected in common to the second and gates respectively connected to the first node and the output terminal,
- wherein drains of the second MOS transistor of first conductivity type and the fourth MOS transistor of second conductivity type are connected in common, drains of the third MOS transistor of first conductivity type and the fifth MOS transistor of second conductivity type are connected in common, and the drain of the second MOS transistor of first

conductivity type is connected to the gate of the second MOS transistor of first conductivity type.

12. (Currently Amended) The circuit according to claim 10, wherein the second switch comprises second and third ~~sixth and seventh~~ MOS transistors of second conductivity type connected in series, and the third ~~seventh~~ MOS transistor of second conductivity type is connected at a gate thereof to the output terminal.

13. (Currently Amended) The circuit according to claim 12, wherein the first switch comprises a fourth ~~an eighth~~ MOS transistor of first conductivity type, and gates of the ~~eighth~~ fourth MOS transistor of first conductivity type and the ~~sixth~~ second MOS transistor of second conductivity type are connected in common.

14. (Original) A noise filter circuit comprising the delay circuit recited in claim 10.

15. (Original) The circuit according to claim 12, further comprising:
an input pad connected to an input end of the delay circuit; and
a logic circuit having a first input end connected to an output end of the delay circuit and a second input end connected to the input pad.

16. (Original) The circuit according to claim 15, wherein the logic circuit comprises a NOR circuit.

17. (Original) A delay circuit comprising:

a first transistor of first conductivity type connected between a first power supply and a first node, the first transistor being switched according to an input signal;

a second transistor of second conductivity type having a current path connected at a first end thereof to the first node, the second transistor being switched according to the input signal;

a third transistor of second conductivity type connected between a second end of the current path of the second transistor and a second power supply, the third transistor making a constant current flow according to a control signal formed of a constant current;

a capacitor connected between the first node and the second power supply; and

a differential amplifier supplied at a first input end thereof with a potential at the first node and supplied at a second input end thereof with a potential depending upon the control signal, the differential amplifier comparing the potential at the first node with the potential depending upon the control signal and outputting an output signal from an output terminal thereof.

18. (Currently Amended) The circuit according to claim ~~15~~ 17, the differential amplifier comprising:

a fourth transistor of first conductivity type having a current path connected at a first end thereof to the first power supply;

a fifth transistor of second conductivity type having a current path connected at a first end thereof to a second end of the fourth transistor and connected at a second end thereof to the second power supply, the fifth transistor being connected at a gate thereof to the first input end;

a sixth transistor of first conductivity type having a current path connected at a first end thereof to the first power supply, the sixth transistor being connected at a gate thereof to a gate of the fourth transistor and a second end of the current path of the fourth transistor; and

a seventh transistor of second conductivity type having a current path connected at a first end thereof to a second end of the sixth transistor and connected at a second end thereof to the second power supply, the seventh transistor being connected at a gate thereof to the second input end.

19. (Original) The circuit according to claim 17, further comprising a constant current source circuit for generating the control signal formed of the constant current.

20. (Original) The circuit according to claim 19, the constant current source circuit comprising:

a first current mirror circuit;

a fourth ~~an eighth~~ transistor of first conductivity type having a current path connected at a first end thereof to the first power supply, the fourth ~~eighth~~ transistor being connected at a gate thereof to an output node of the first current mirror circuit; and

a fifth ~~ninth~~ transistor of second conductivity type having a current path connected at a first end thereof to a second end of the fourth ~~eighth~~ transistor, the fifth ~~ninth~~ transistor being connected at a second end of the current path to the second power supply, the fifth ~~ninth~~ transistor being connected at a gate thereof to the second end of the fourth ~~eighth~~ transistor, a gate of the third transistor, and the second input end of the differential amplifier,

the fourth ~~eighth~~ transistor and the fifth ~~ninth~~ transistor forming a second current mirror circuit, the second mirror circuit making a current equivalent to an output current of the first current mirror circuit flow.

21. (Original) A noise filter circuit comprising the delay circuit recited in claim 17.

22. (Original) The circuit according to claim 21, further comprising:

an input pad connected to an input end of the delay circuit; and

a logic circuit having a first input end connected to an output end of the delay circuit
and a second input end connected to the input pad.